REMARKS

Claims 1, 3, 5-7, 11-17 and 20-22 are pending in the application.

Claims 1, 3, 5-7, 11-17 and 20-22 had been rejected.

Reconsideration of the Claims is respectfully requested.

1. Rejection under 35 USC § 103

Claims 1,3,5-7, 11-17, 20, 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over US Published Application 2002/0183013 to Auckland et al ("Auckland"), in view of US Patent No. 5968143 to Chisholm et al ("Chisholm"), and further in view of U.S. Patent No. 6,434,630 to Micalizzi Jr, et al ("Micalizzi").

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142, p. 2100-128 (Rev. 2, May 2004) (citations omitted).

Auckland relates to an "analog RF hardware in the front ends of personal and mobile communication radios that is reconfigurable for a variety of air interface standards." (Auckland ¶ 0048). In this regard, Auckland generally recites *memory in an operational usage* for RF portion 600 configurations, which includes a "controller 614 may be dedicated to controlling the RF front end of the radio, including functions such as modulation, demodulation, encoding and decoding. In a software definable radio, where the radio hardware is fixed but may be customized by on-board *software during operation to allow the radio to operate in conjunction with a particular air interface standard or on a particular frequency band, the customization operation may be controlled by the controller 614.*" (Auckland ¶¶ 0077, 0090; *see* Figure 6) (emphasis added).

The Office Action mailed January 23, 2006, noted that "Auckland does not describe the memory structure for storing addresses for accessing data blocks." (Office Action mailed January 23, 2006 at p. 7). Further, Auckland pays passing, if any, attention to data access. Instead, Auckland recites antenna configuration techniques (see, e.g., Auckland Claim 1), and radio configuration techniques (see, e.g., Auckland Claim 15; cf. Auckland ¶ 0143 ("Other components of the radio may access data in the memory

over a system bus or other communication means."). Accordingly, Applicant respectfully submits that the Office Action uses the radio corollary in Auckland, but lacks a corollary for memory data access.

Chisholm relates to "transfer of command blocks between two processing units communicating over an expansion bus." (Chisholm 1:16-17). In this regard, Chisholm's Summary of the Invention recites a "*command block transfer controller* [that] is *responsive to the transfer start signal* written by the host processing unit to start a command transfer for retrieving a command block from a corresponding host memory portion without local processing unit intervention." (Chisholm 3:1-4) (emphasis added).

But the device of Chisholm relates to the handling of the command blocks, not data, to local processing sides within a personal computer. For example, Chisholm recites that "[during] a *command block transfer* from the host processing side 110 to the local processing side 120, the FIFO buffer 326 receives and temporarily stores the *command block* from the host DMA state machine 322 and provides such *temporarily stored command block* to the local DMA state machine 324 to be stored in a *command block portion* of the local memory." (Chisholm 5:16-22).

Further, the command block of Chisholm "includes a command portion and a command address portion appended thereto." (Chisholm Claim 2). The "command address portion includes a chain enable information indicating whether another command block is chained to the transferred command block." That is, Chisholm *does not address* data transfer. Further, the dissimilar command blocks of Chisholm do not include addresses of data blocks stored within random access memory and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in use.

Micalizzi relates "to a host adapter which reduces the number of input/output (I/O) completion interrupts generated from the host adapter to a host microprocessor." (Micalizzi 1:9-12). That is, Micalizzi is a device to increase processor performance by "combining successful I/O completion reports and reducing the number of interrupts, the host adapter reduces the overhead incurred in servicing interrupts for successfully completed I/O requests. This reduces the amount of processing time (`I/O bound` time) and power spent by the host microprocessor in *processing interrupts from the adapter*, and creates more time and power for the host microprocessor to *process user applications*. In one embodiment of the present invention, the amount of time and/or resources (e.g., power) spent by the host microprocessor in servicing interrupts (CPU utilization) is decreased by 20%." (Micalizzi 2:5-15). Micalizzi does not address command blocks with addresses of data blocks and indicators for command blocks.

In contrast, Applicant's Independent Claim 1 recites, *inter alia*, a "*wireless transceiver device*, comprising: . . . a plurality of command blocks formed within a memory structure, the command blocks *include addresses of data blocks* stored within random access memory and a memory portion for storing *an indicator* for indicating whether a command block of the plurality of command blocks is in use." (emphasis added).

Applicant's Independent Claim 7 recites, *inter alia*, a "method for storing and transmitting data, comprising: . . . storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure, the pointer includes an address of a command block; storing an address of the data block in the command block; and *setting an indicator signal* in a defined memory location, wherein the indicator signal indicates that the data block address stored in the command block is for data *that has yet to be successfully transmitted and that the command block is busy*." (emphasis added).

Applicant's Independent Claim 17 recites, *inter alia*, a "memory structure formed within a baseband processing system, comprising: a random access memory portion for storing data blocks that are to be transmitted in a first in, first out (FIFO) order; and a FIFO memory structure for storing pointers that correspond to the data blocks stored in the random access memory portion; a plurality of command blocks defined within the random access memory portion wherein *each command block is for specifying an address of a data block that is to be transmitted*; and a defined memory portion for storing *command block indicators* for each command block, wherein the command block indicators specify whether its corresponding command block includes the address of a data block that has yet to be transmitted successfully." (emphasis added).

Applicant respectfully submits that a *prima facie* case of obviousness has not been set out. There is no suggestion or motivation to modify the reconfigurable RF front end of Auckland with the command block transfer of Chisholm, and further with the interrupt reduction of Micalizzi to achieve Applicant's claimed invention. Further, the cited references do not teach or suggest all the limitations of Applicant's claimed invention. Applicant respectfully requests that the rejection to Independent Claim 1 and Claims 2, 5, and 6 that depend therefrom, to Independent Claim 7 and Claims 11-16 that depend directly or indirectly therefrom, and to Independent Claim 17 and Claims 20-22 that depend directly or indirectly therefrom, be withdrawn.

2. Conclusion

As a result of the foregoing, the Applicant respectfully submits that Claims 1, 3, 5-7, 11-17, and 20-22 in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *ksmith@texaspatents.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126 (Reference BP 1907).

Respectfully submitted,

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